PINGU DOM Design "PDOM"

Perry Sandstrom

VLVnT conference Stockholm

August, 2013

Outline

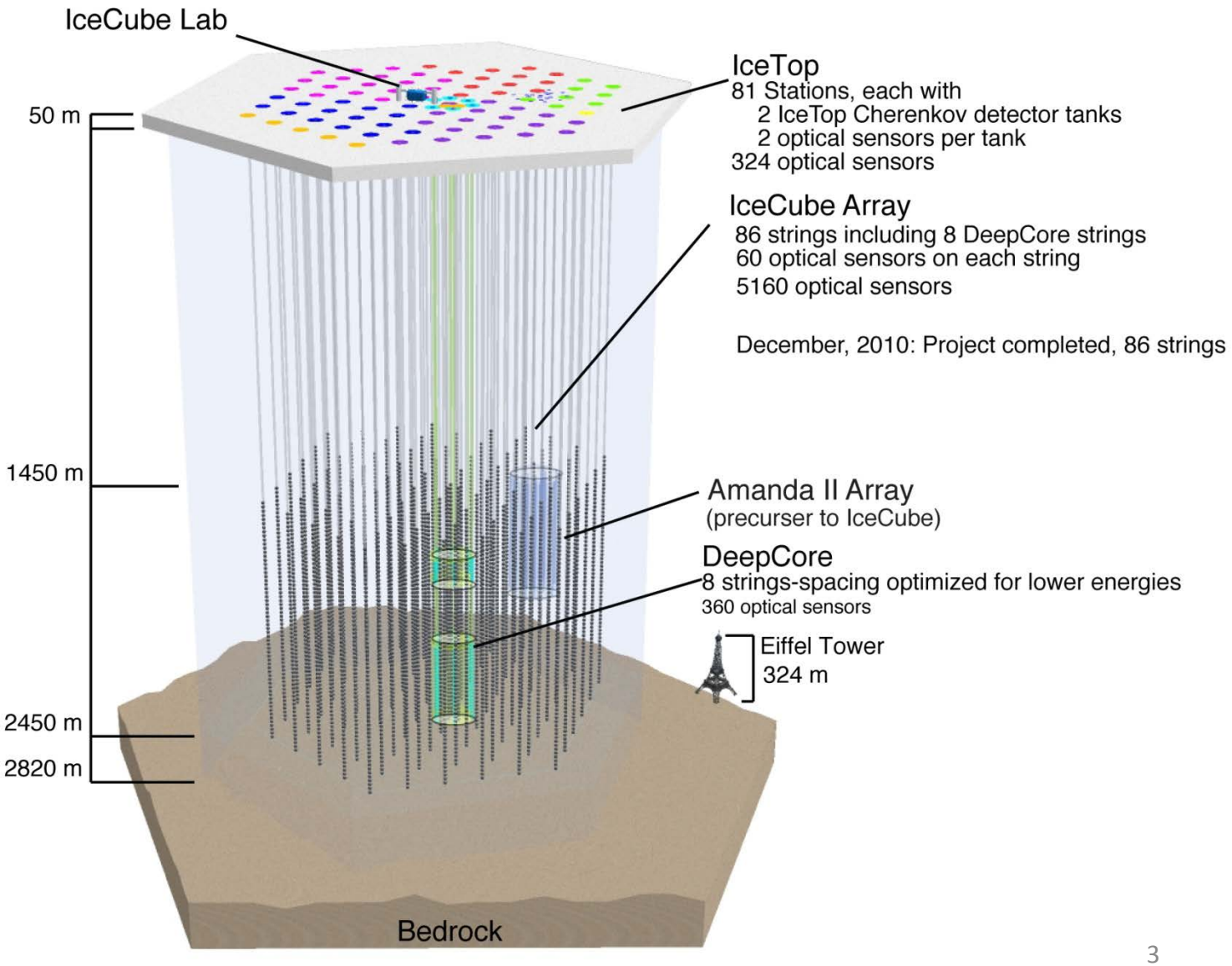
- Detector Requirements / IceCube Overview
- Departures from IceCube
- Detector and PDOM Functional Blocks
- Prototyping Plan
- Discussion

With Many Thanks to:
Kyle Jero, Chris Wendt, John Kelly, Andrew Laundrie, Albrecht Karle, Jim Haugen, Mike Duvernois, Kael Hanson, Jerry Przybylski, Thorsten Stezelberger, Sebastian Boser Arthur Jones, Dave Nygren, Doug Cowen, Darren Grant, Elisa Resconi, Ty DeYoung, Jean DeMerit.

IceCube

7 drilling seasons at Pole(colored dots)

- Total of 86 strings and 162 IceTop tanks;
- Completion with 86 strings: December 2010
- Full operation with all strings since May 2011.
- > 99% uptime
- ~99% DOM Survival
- No known pressure vessel failures



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South Pole 10m Telescope

IceCube Counting Laboratory (ICL)

Drilling site

IceCube Enhanced Hot Water Drill (EHWD)

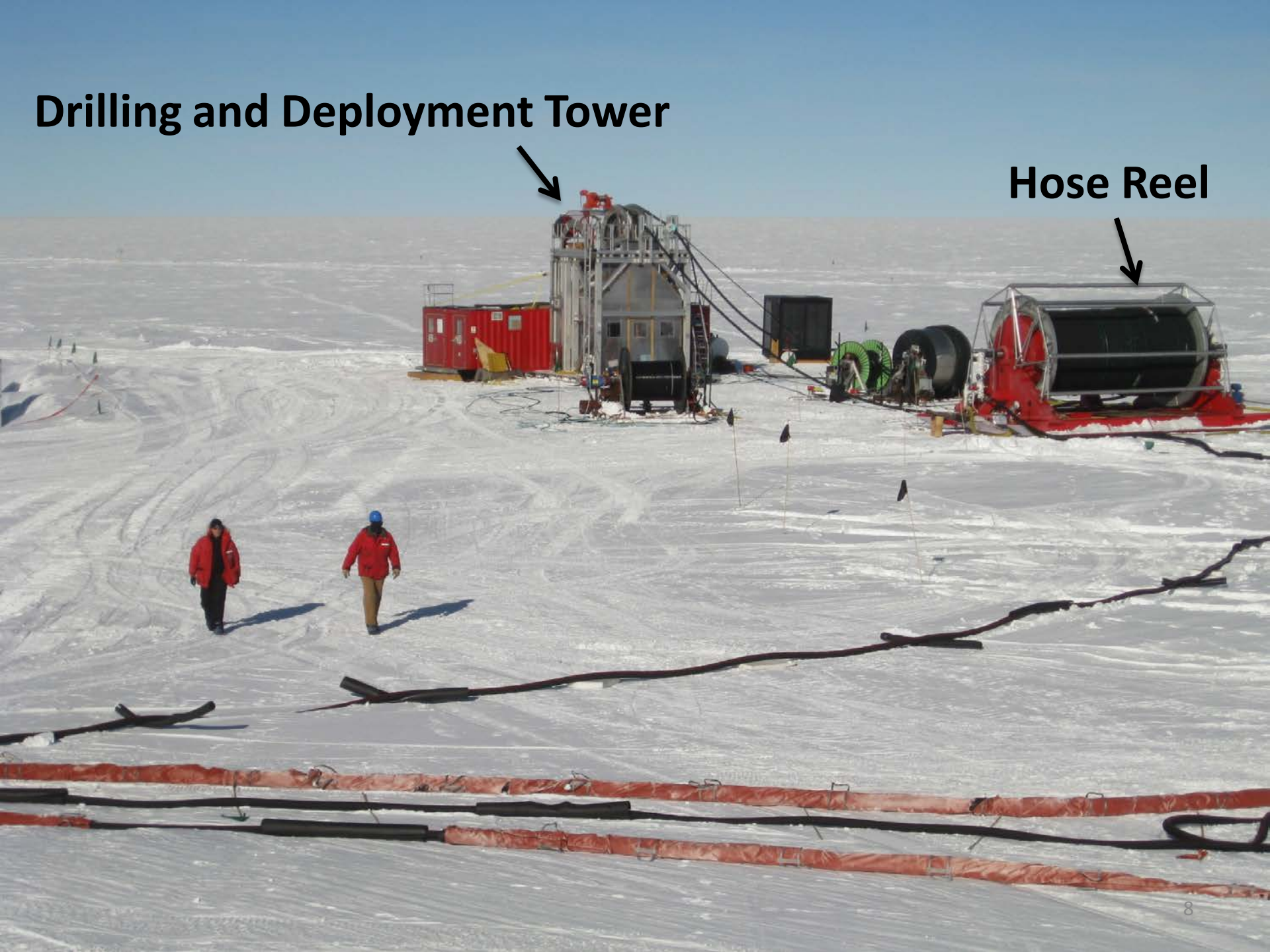
PINGU
System Engineering Targets

- Angular Acceptance — Same as IC
- Sensitivity — = High QE DOMs in IC
- Timing Resolution — <= IC
- Dynamic Range — comparable to IC
- Background Rate — Same as IC (High QE)
- Local Coincidence — No Hard-wired Local Coincidence
- Avg. DOM Data Rate — ~ Same as IC
- DOM Spacing — < IC (~5m vs 17m)
- # DOMS per string — 60-120
- #Strings — ~20-40
- Depth/Environment — same as IC

U and T DOMs ready to deploy

Main Design Departures from IceCube

- Mechanical:
  - Possible Link-Link deployment of “PDOMs” (no cable “bow”)
  - Same or smaller cross-section cable for ICL entry
- Electrical:
  - Double the number of DOMS per Wire-pair
  - No “U” and “T” DOM Types; termination in breakout cable
  - No Hard-wired LC; simpler down-hole cable assembly, lower noise
- New DOM Mainboard
  - Continuous (~200MHz) commercial ADC digitizer w/ FPGA trigger
  - Reduce Power by half (~2W target)
  - Possibly enhanced communications scheme (PSK, QAM, QPSK)
  - Possibly integrate flasher, HV, Camera, other, onto mainboard
- New Hub Design Expected (needs discussion)
  - IceCube compatibility (backwards/forwards)


Drilling and Deployment Tower
Hose Reel

Deploying IceCube DOMs

Strawman String Design

Harness–Link-Link–Harness

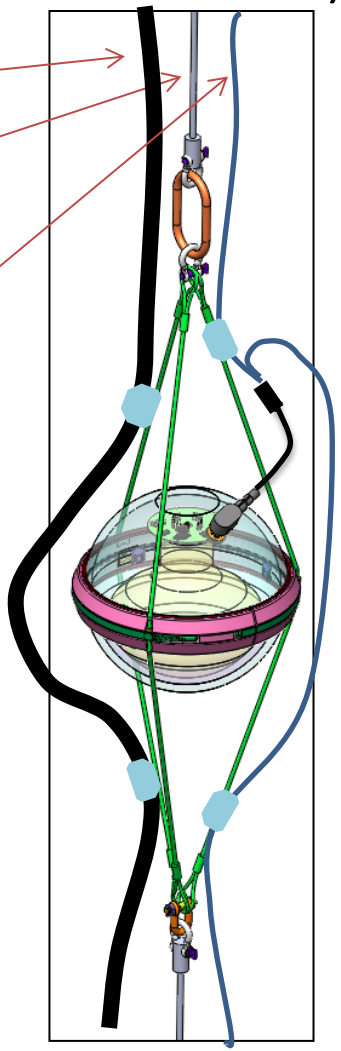
Possible elimination of cable bow at each DOM

(Baseline remains IceCube-Like deployment with cable bow)

Downhole Cable Assembly (DCA)

NEW: Link (3/8” SS wire rope)

NEW: Breakout Cable Assembly (BCA)



Incremental Deployment:

-DOM, Link, Link, DOM, Link, Link, etc

-Use single winch in TOS

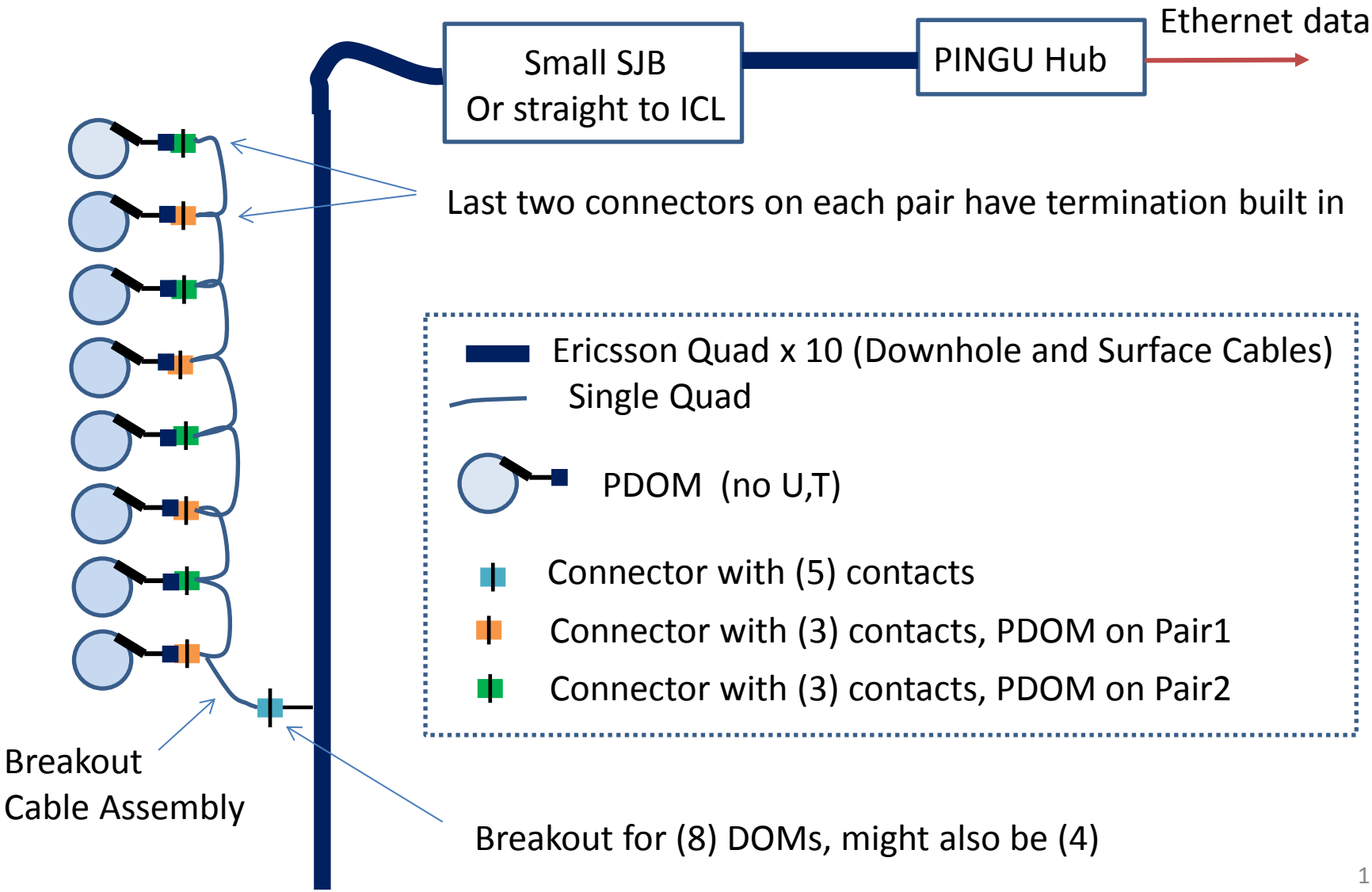
- Single link for smaller spacings

-Downhole Cable for final Drop

Minimum spacing with current harness: 1.5m

Possible Cable System Architecture

Elimination of Hard LC reduces breakout complexity

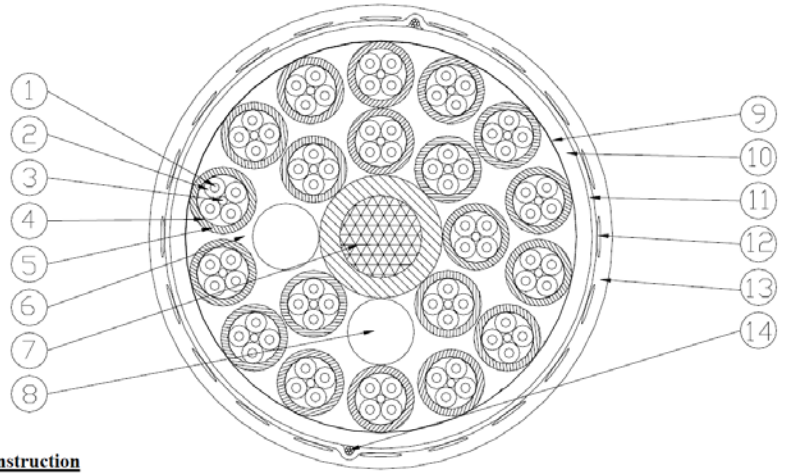


IceCube Raw Down-hole Cable

Baseline Design for Pingu, but Ericsson closing this factory (!)

- (20) Quads
- Inner/outer strength members
- AWG 19 conductors, 0.025 Ω/m
- Z=~145Ω, Loop R= 120 Ω
- Precision Low cross-talk design:
  - -50dB intraquad & quad-quad @2MHz
- Low attenuation:
  - -20dB attenuation over 3km
- 1Mb/s nominal BW using ASK

Ericsson product code: **TEH 301 9099/0040**
Type designation: **ELLLZIV 20x4x0.9**



Construction

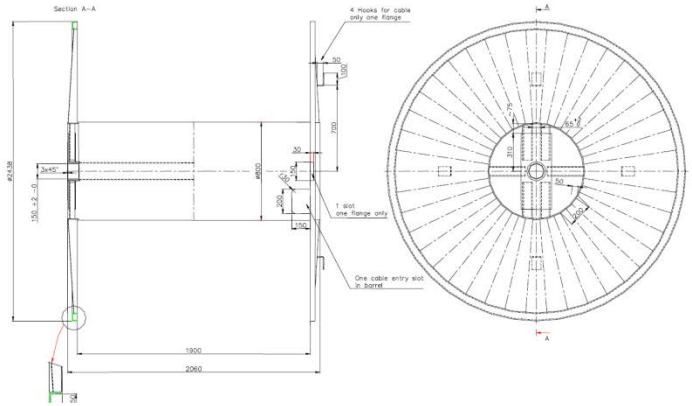
Quads 20 units

Description		Material	Diameter	Unit
1	Conductor	Copper wire solid	0.9	mm
2	Insulation	PE, solid	2.1	mm
		Pair Colour		
		1 white, blue		
		2 turquoise, violet		
3	Filler	PE-Thread	0.9	mm
4	Wrapping (optional)	Plastic tape or chalk (to prevent adhesion)		
5	Sheath	PE-LLD ,Colour black, thickness =0.5 mm	6.5	mm
6	*Filling compound*	Polybutene based jelly		
7	Strength member	PE-sheathed aramid yarn	12	mm
8	Filler	PE	6.5	mm

Finished cable

Description		Material	Diameter	Unit
9	Outer wrapping	Laminated plastic tape thickness =0.25mm		
10	Sheath	PE-LLD ,Colour black thickness = 2 mm	42	mm
11	Shield	Copper tape thickness =0.1 mm	42.5 ±0.5	mm
12	Strength member	Aramid yarn		
13	Sheath	TPE-U , Colour black thickness =1.8 mm	46 ± 1	mm
14	Drain wires	Tinned stranded copper wire 7x0.30mm	0.9	mm

Drawing of delivery drum



Strawman PINGU “PDOM” Design

Keep these parts/designs:

- Sphere
- Penetrator
- PMT, Collar, Gel
- Harness
- HV generator and Divider
- Quad Cable technology*

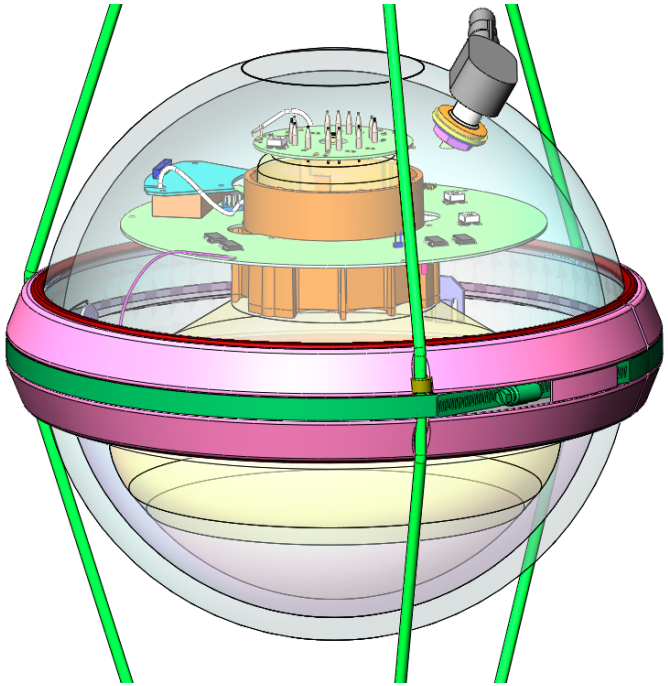
Develop new:

- Digitizer (ADC)
- Front end - shaper
- Comms circuitry
- Flasher
- FPGA logic
- Power Supply
- PCB & packaging
- **Built-in Camera?**

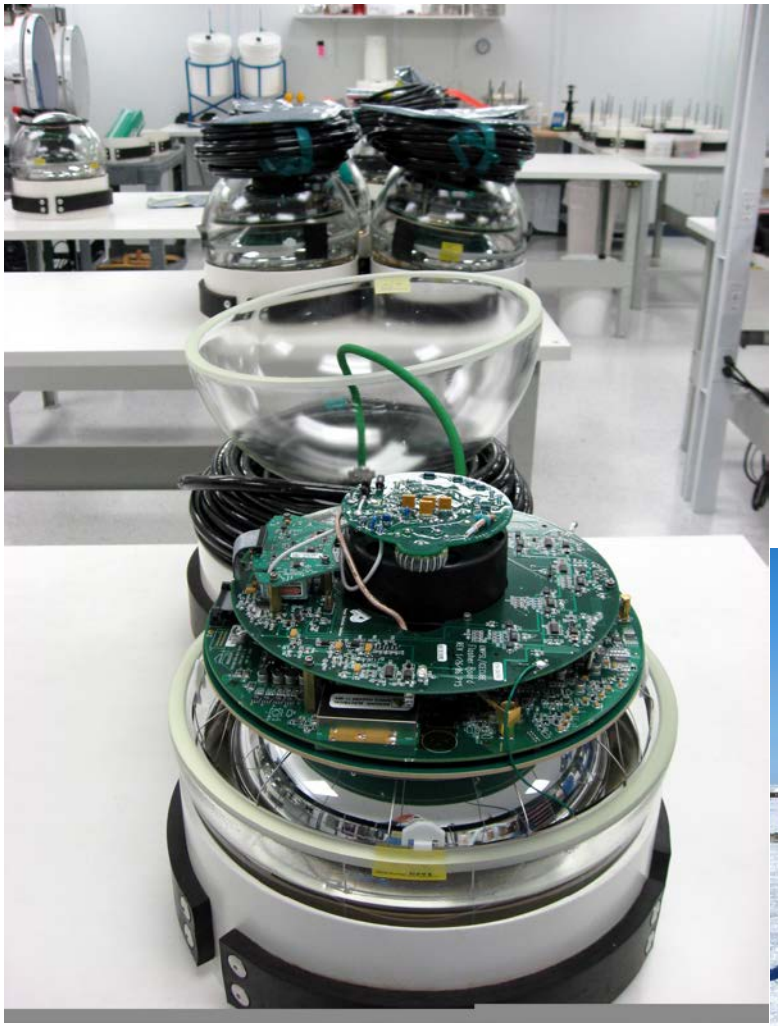
- (PDOMHub- ~2+ new PCBs)

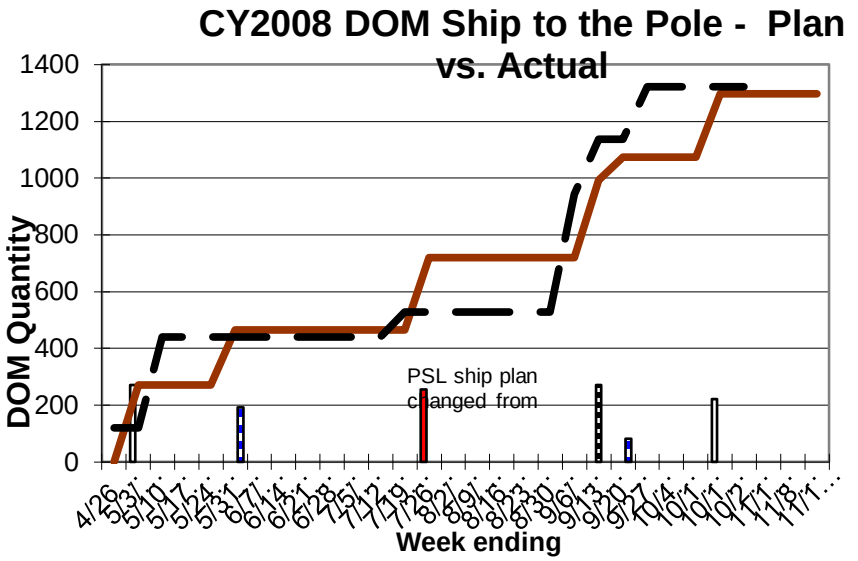
Keep/upgrade these Designs:

- DOMAPP
- CONFIGBOOT (Built into FPGA now)
- DAQ
- DOR FUNCTIONALITY



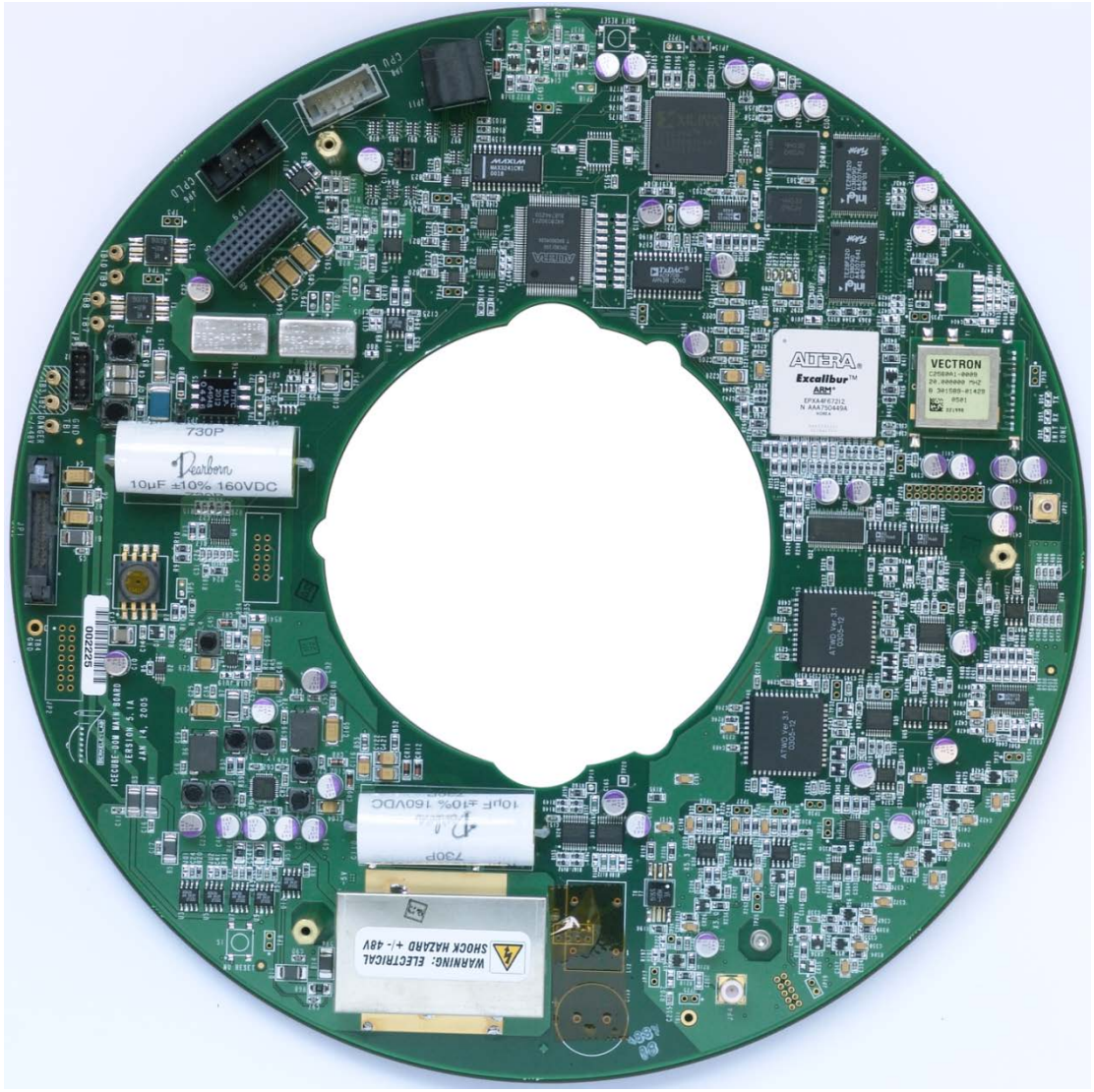
Retain Integration, Testing and Handling





IceCube DOM Mainboard (LBNL)

Quality of this design was a major key to IceCube's success



- High Reliability Components
- Good vendors for PCB assembly
- DFM- Design for Manufacture
- DFT- Design For Test
- Thorough design verification
- Thoughtful revisioning

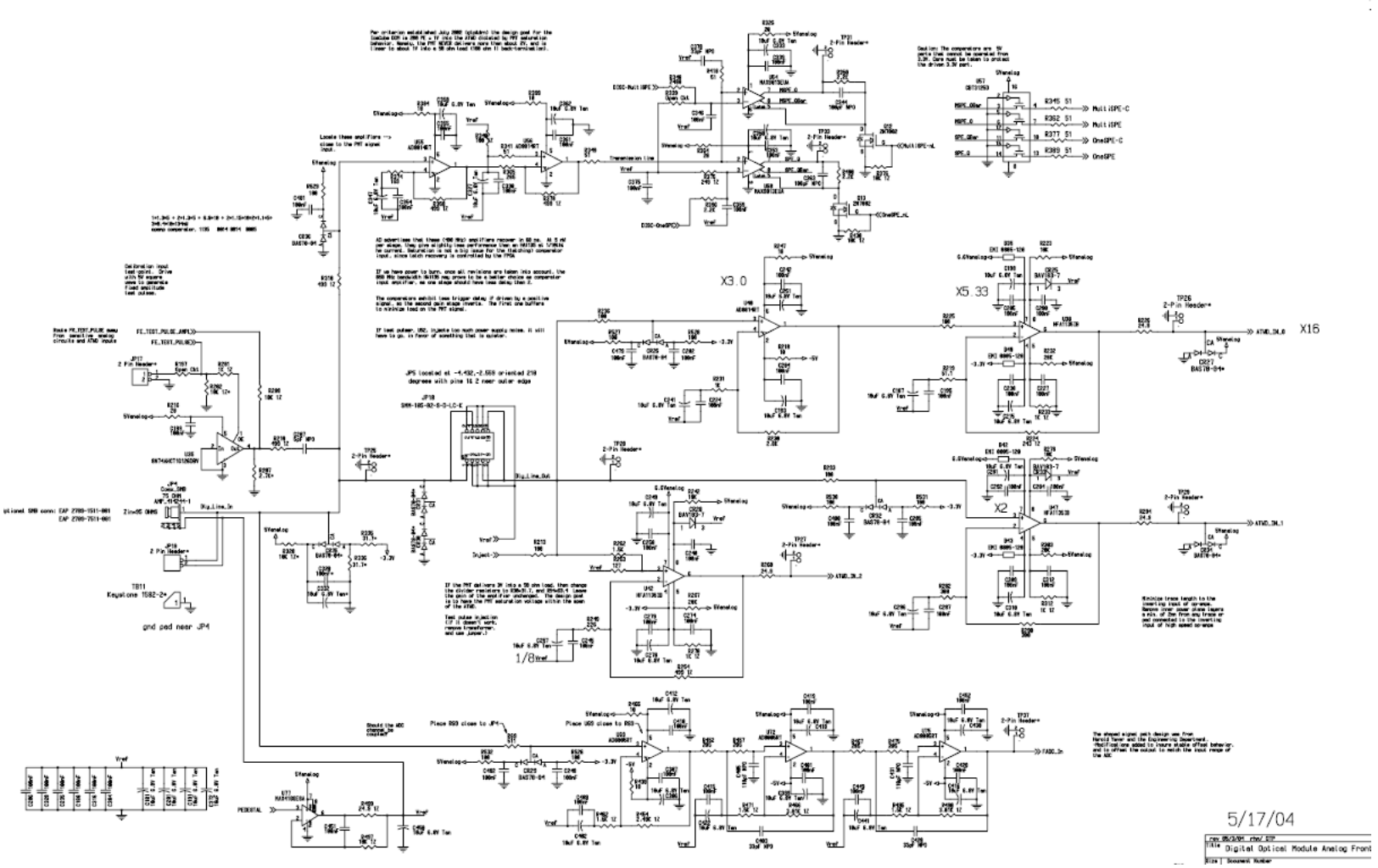
Why mess with proven DOM design?

- ATWDs not guaranteed available
- Obsolete parts, e.g. PSU IC and FPGA
- High Speed ADCs recently available
- Compression of data eliminates need for LC
- More is now known about performance
- Requirements less stringent (dynamic range)

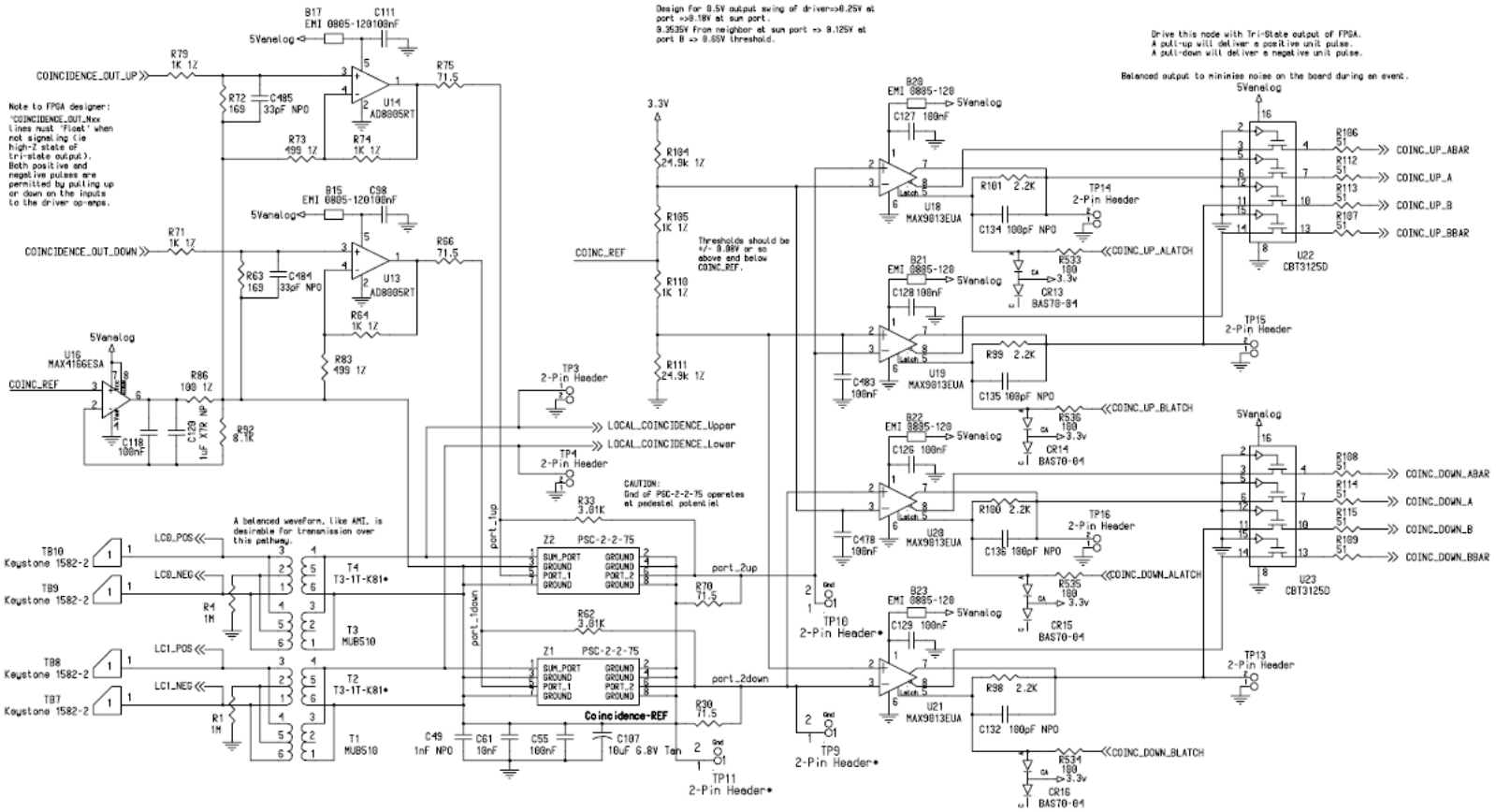
Significant Part Reduction Opportunity

- Updated Design Eliminates:
  - Delay Board
  - Two ATWDs (replace with single ADC)
  - Most Gain Stages
  - Discriminators
  - Local Coincidence (LC) Components

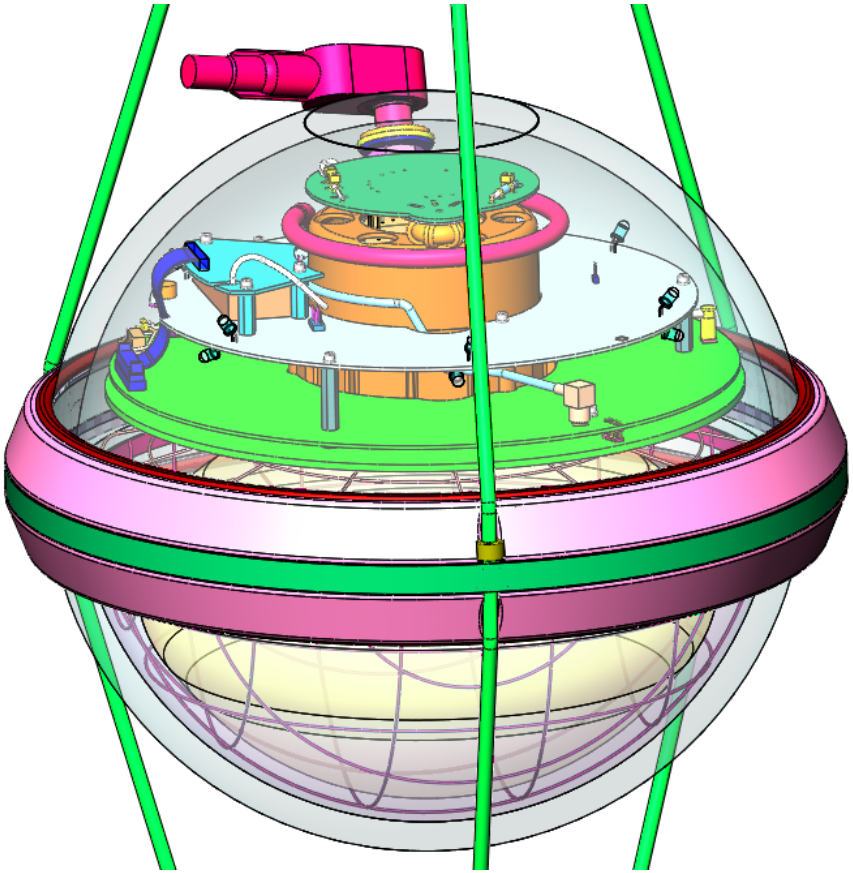
Eliminate Most Front End Circuitry



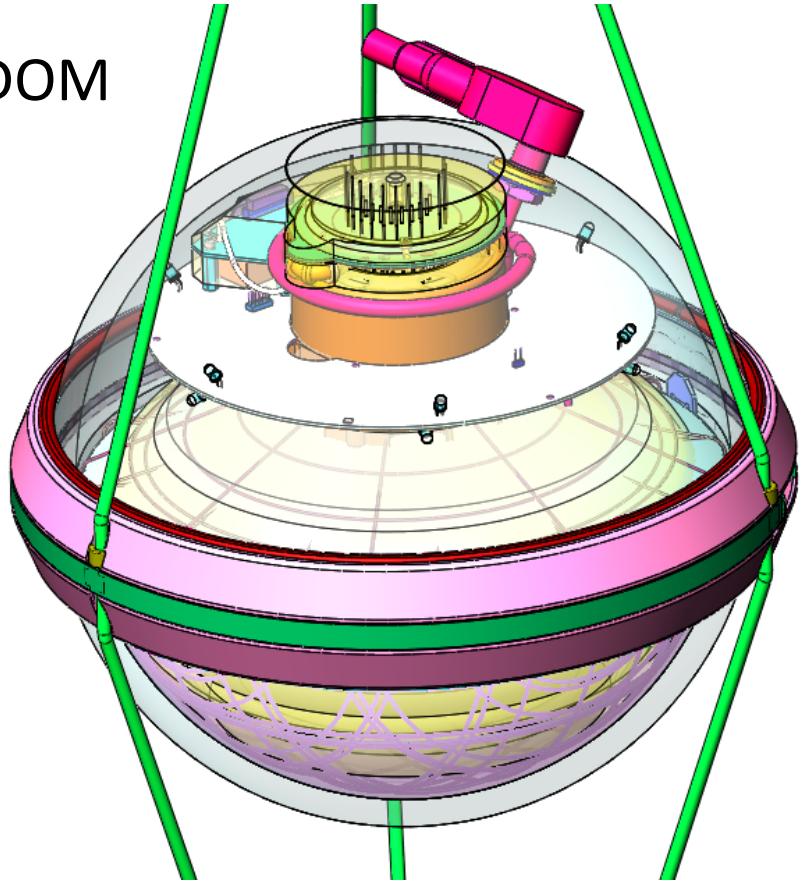
Eliminate All LC Circuitry



IceCube DOM

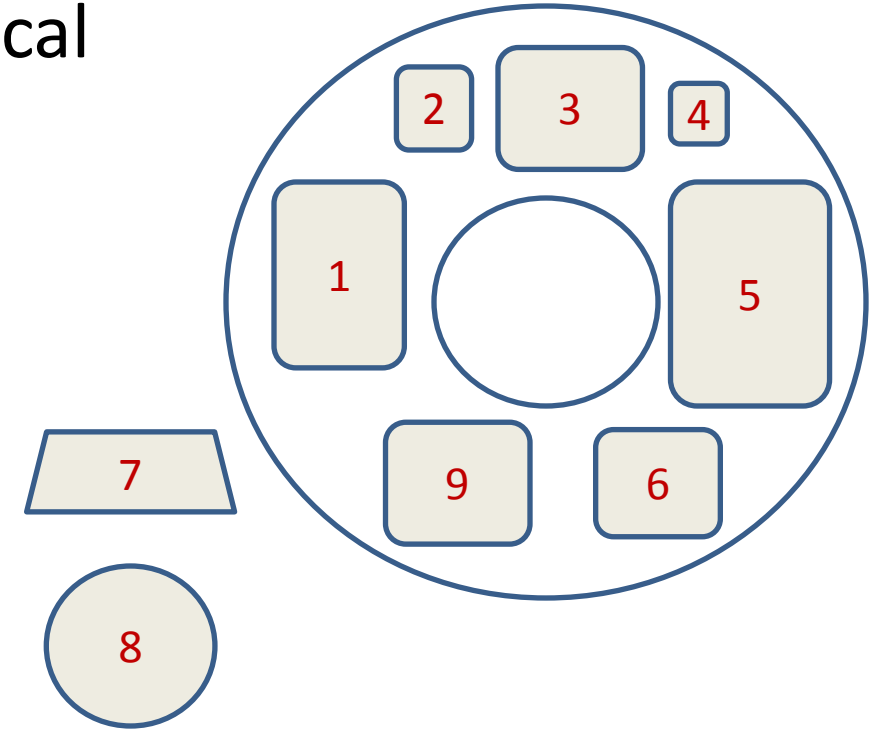


PDOM

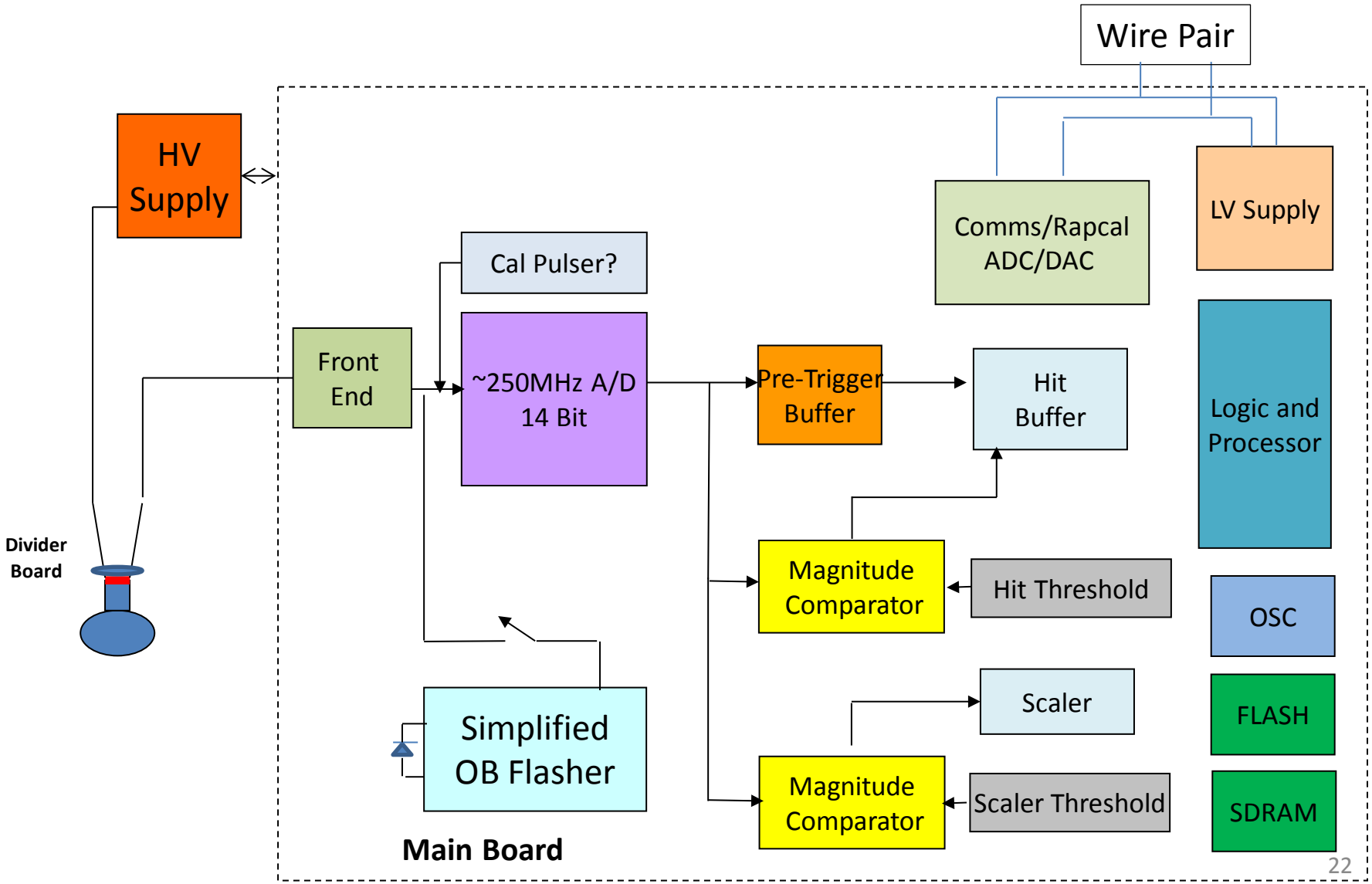


PDOM Electronic Subsystems

1) Digitizer
2) Front End (offset & shaping)
3) Communications/Rapcal
4) Oscillator
5) Logic & Processor
6) LV Supply
7) HV Supply
8) PMT Divider
9) Flasher



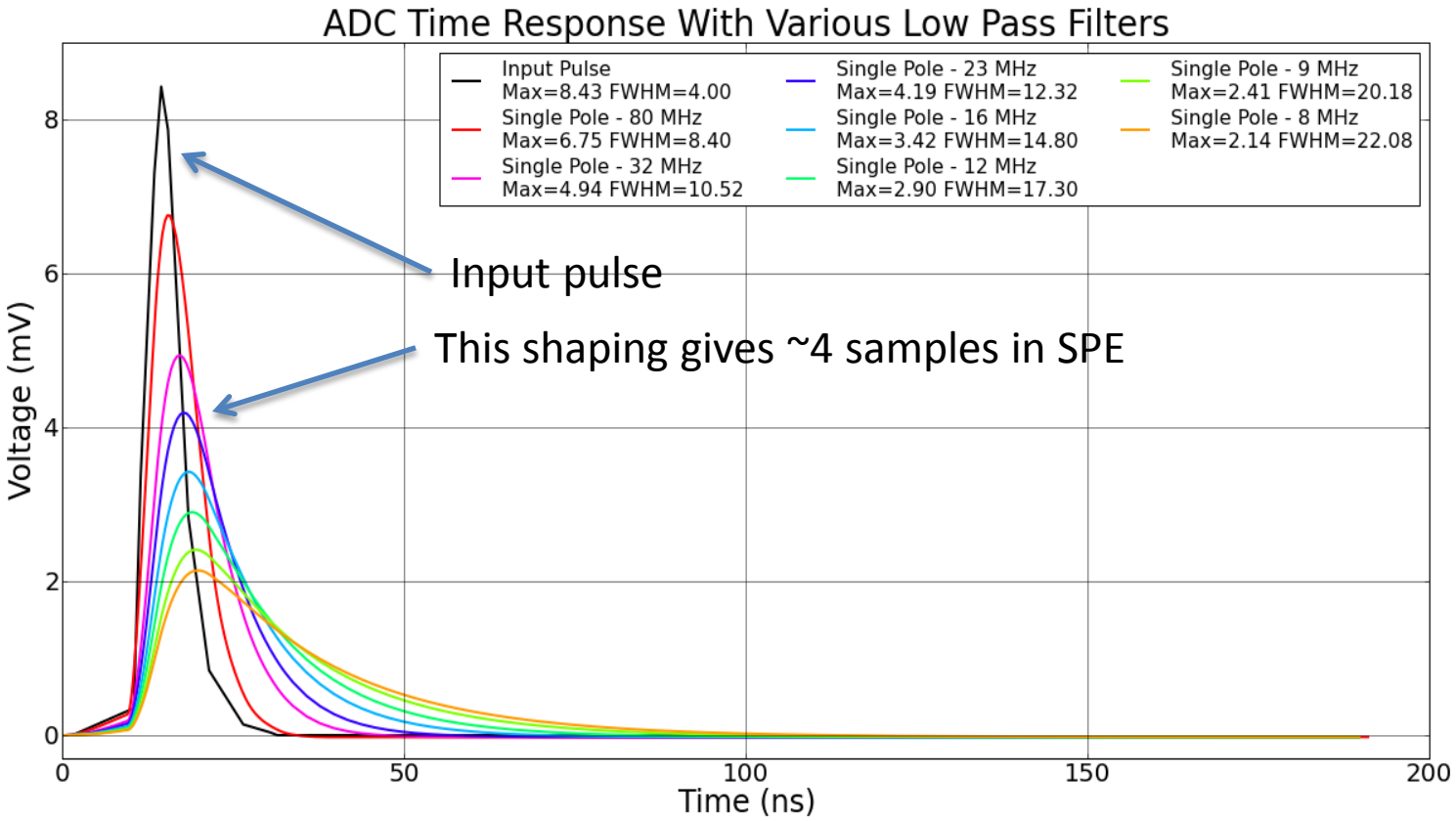
PDOM Block Diagram



Front End Basic Requirements

- Provide DC Offset
  - Use full range of ADC input
  - High BW differential-differential coupling into ADC
- Provide Pulse Shaping
  - Spread SPE pulse over many (e.g. 5-6) samples
  - Retain time resolution of feature-extracted pulses
  - Conserve integrated charge
- Low Power
- As simple as possible
  - Easily and accurately modeled

Front End Pulse Shaping (Simulations)
Goal= ~ 20ns FWHM



Kyle Jero

Digitizer Basic Requirements

- Low Power
  - e.g. < 1W
- Digitizing rate > 200MHz
  - ns timing for SPE with shaping & enough resolution
- Digitizer resolution >= 14 bits
  - Want dynamic range from <1/32 SPE to >500 SPE
- Variable Length Buffer
  - Efficient capture of multiple pulses
- Digital waveform threshold “discriminator”
  - Flexible, low power
- Baseline ADC Choice= Texas Instruments ADS41B29

ADS41B49

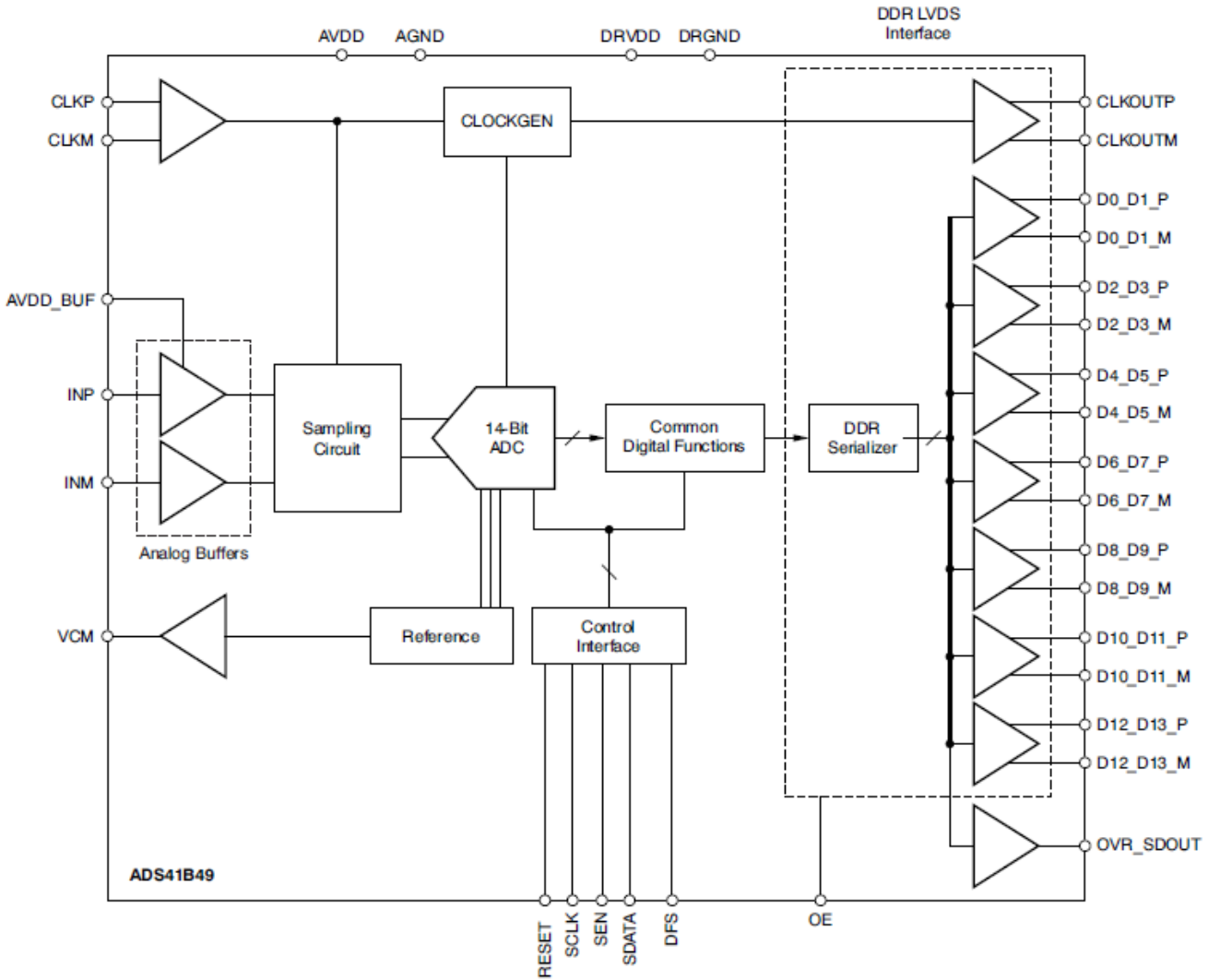
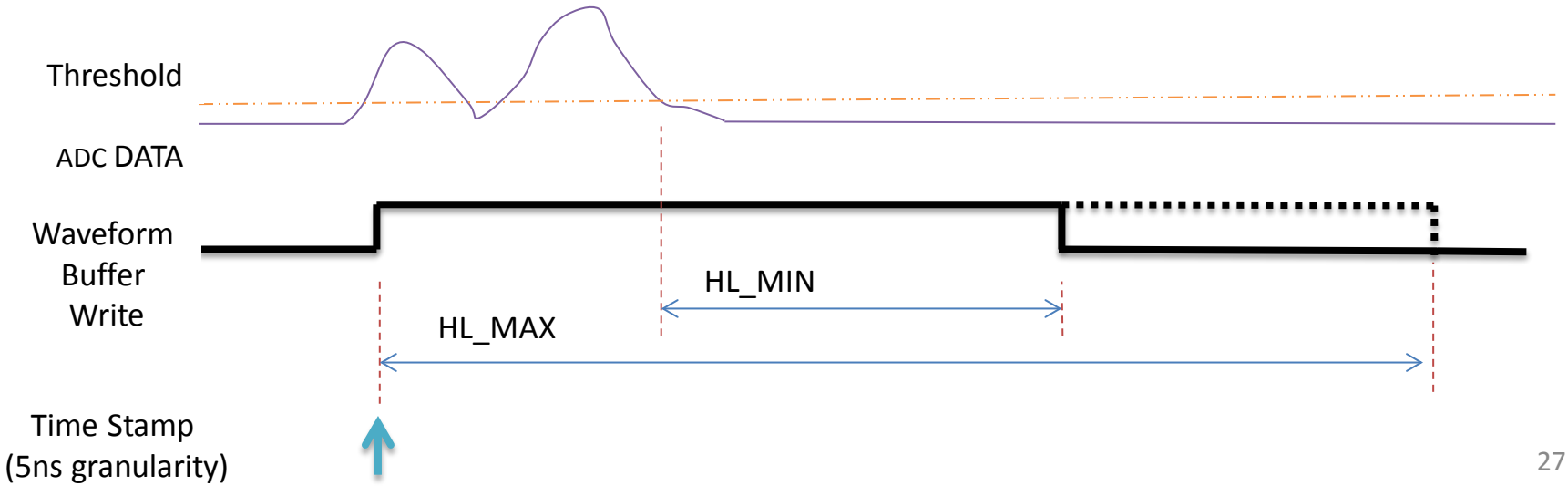


Figure 3. ADS41B49 Block Diagram

- ~1/3W
- 250MS/s
- 14bit
- ~$80
- Buffered input

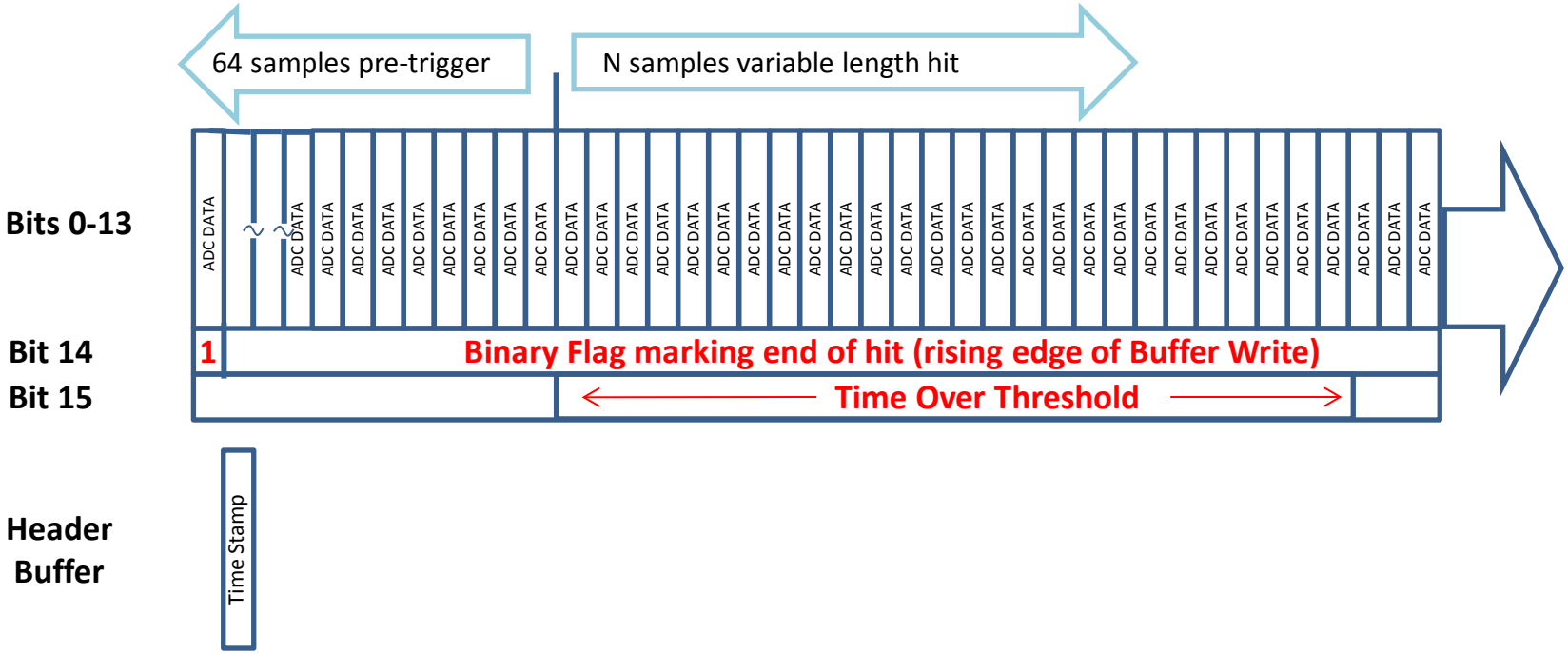
Digitizer Triggering and Buffering

- Always digitizing
- Triggering in firmware (digital comparator) instead of discriminators
- Two Buffer sections:
  - Pre-trigger buffer (e.g. 64 samples, FIFO, replaces delay board)
  - Waveform buffer (e.g. 16K samples, multi-hit, replaces LBM)
- Buffer cells always filled with no dead time (state machine)
- Variable Length Hits :
  - Triggered at threshold crossing
  - Retriggered (counter reset) while ADC DATA > Threshold
  - Min and Max Hit Lengths are programmable (HL_MIN, HL_MAX)



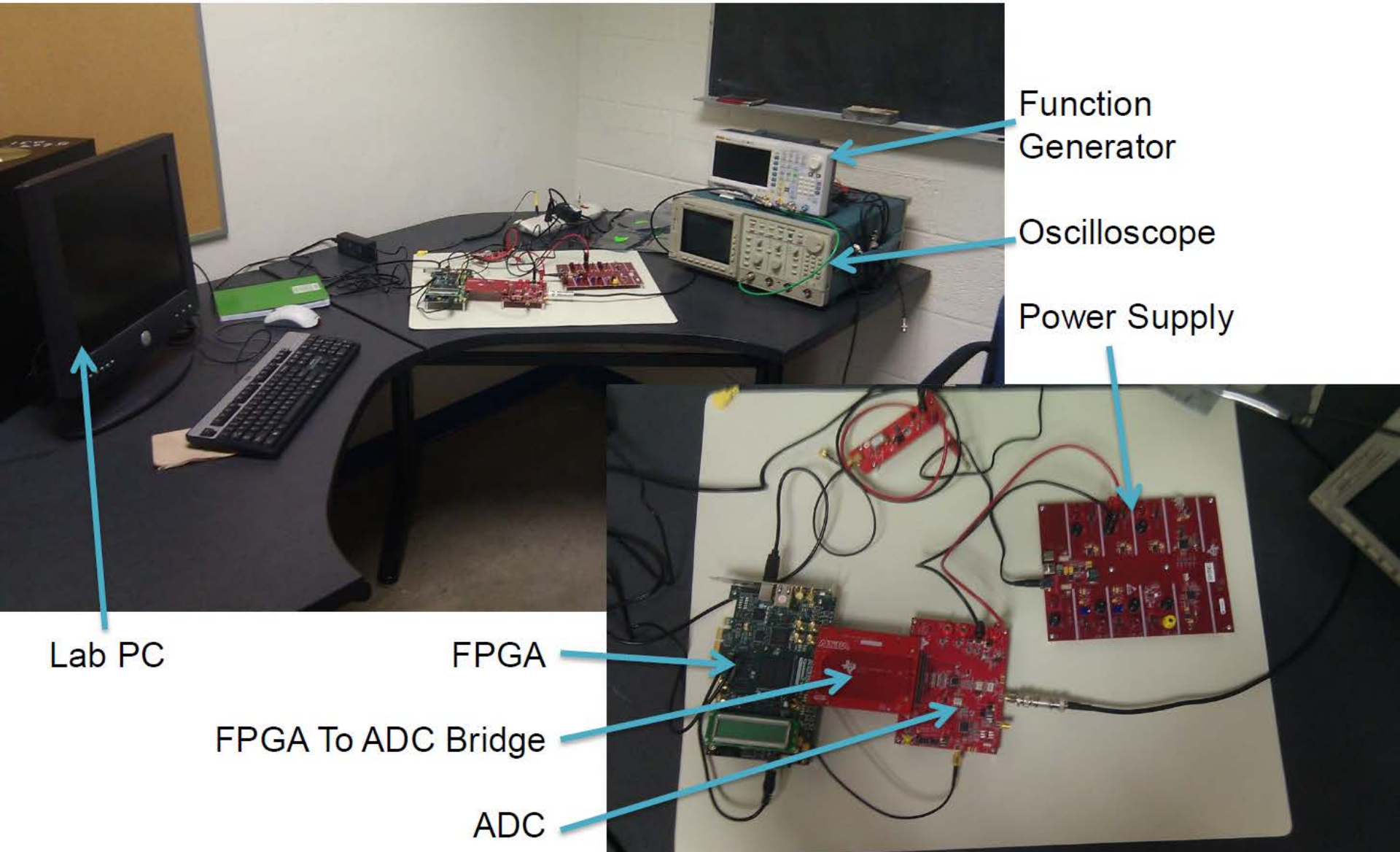
Digitizer Waveform Buffer Format

- Waveform buffer is written synchronously with ADC sampling
- ADC Data is 14 Bit
- FPGA optimal memory width is 20 Bit
- Data stored as 14 bit parallel words
- Time stamp buffered in separate “Header Buffer”
- Simple Binary Flag used to indicate end of hit
- Time-Over Threshold stored
- Hits packaged when waveform buffer transferred to readout buffer

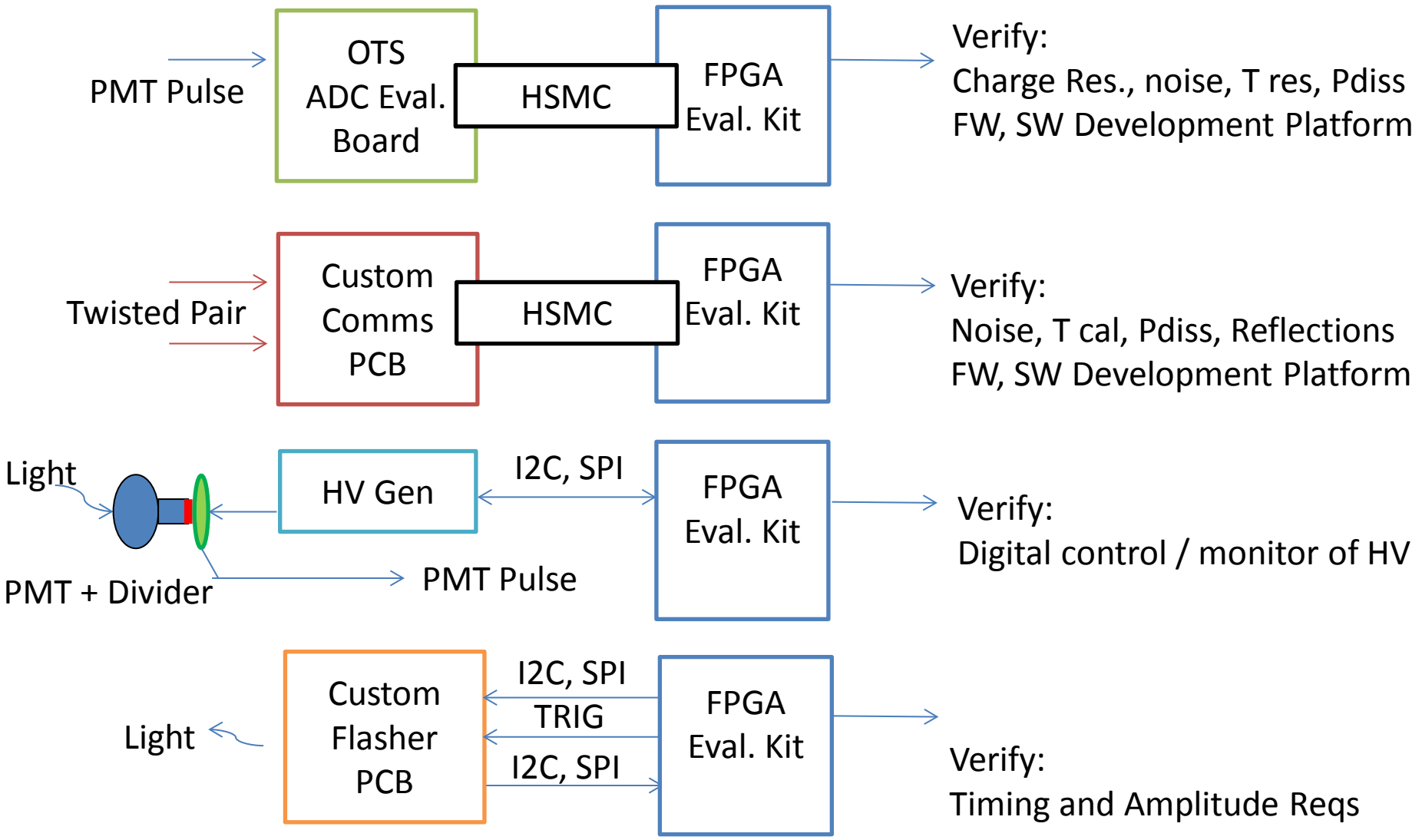


Digitizer: Proof of Concept w/ Eval Kits

Using Altera Cyclone V FPGA and TI AD41B49 250MS/s 14B ADC



Near-term PDOM Prototyping Plan



Weekly PINGU Hardware Call

Currently at 9:00am US Central Thursdays

The docushare location of materials for the call is always here:
https://docushare.icecube.wisc.edu/dsweb/View/Collection-11457

The shadow PINGU wiki page for this call is always under here:
https://wikispaces.psu.edu/display/PINGU/2013+PDOM+Calls

The minutes from each call will also be placed in the above locations.

The DIAL IN information will always be the following:

1 (888) 291-0310 US Toll Free
1 (630) 785-5805 US Toll
Pass code: 6065 798#

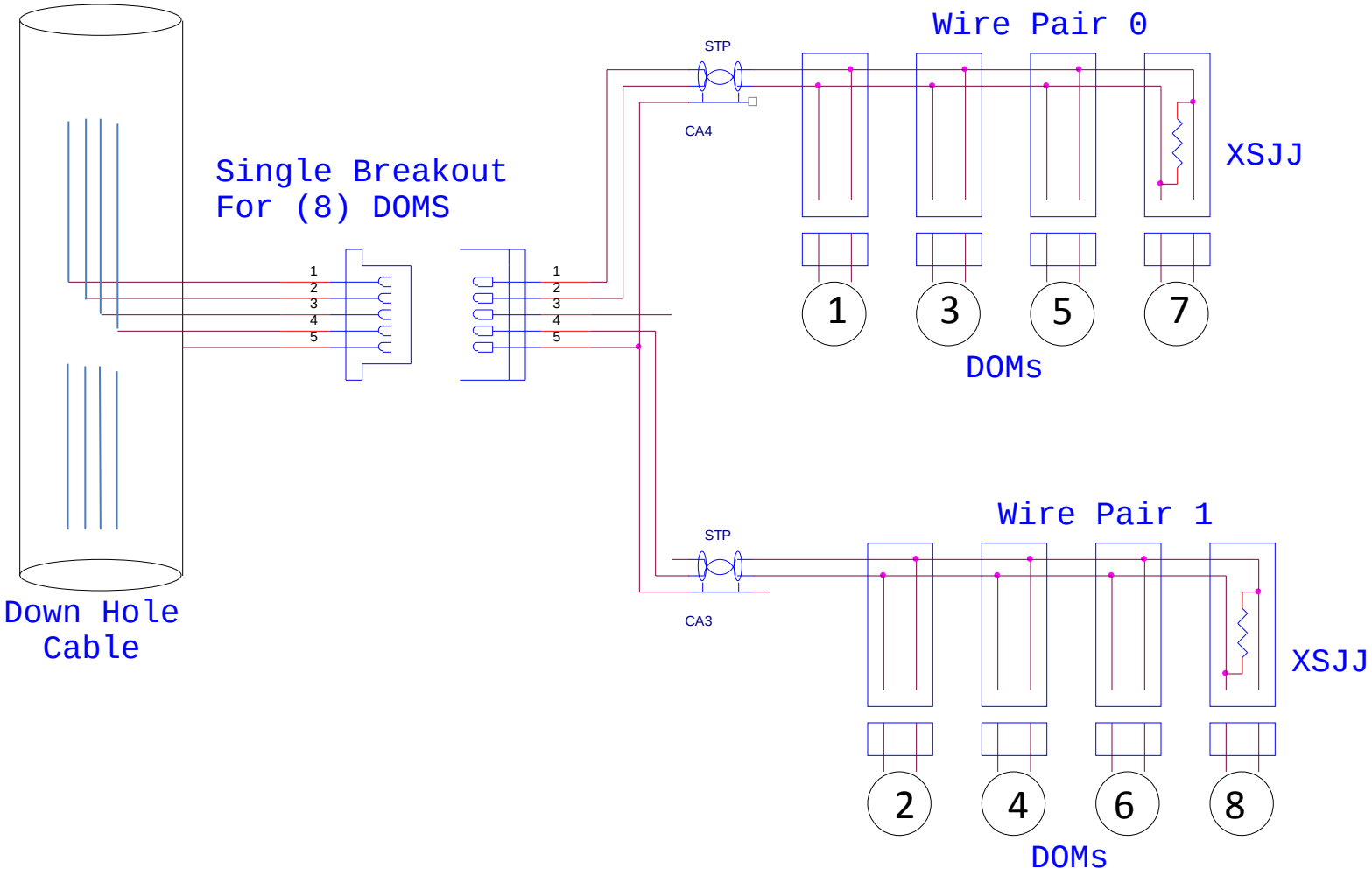
For a current list of available local and international freephone telephone numbers
https://www.yourconferencecenter.com/AlternateNumbers/alternatenumbers.aspx?100761&t=A&o=UMAIZQBTFENJGF

Mailing List:
Pingu-hw@icecube.wisc.edu
To subscribe:
http://lists.icecube.wisc.edu/mailman/listinfo/pingu-hw

Tack!

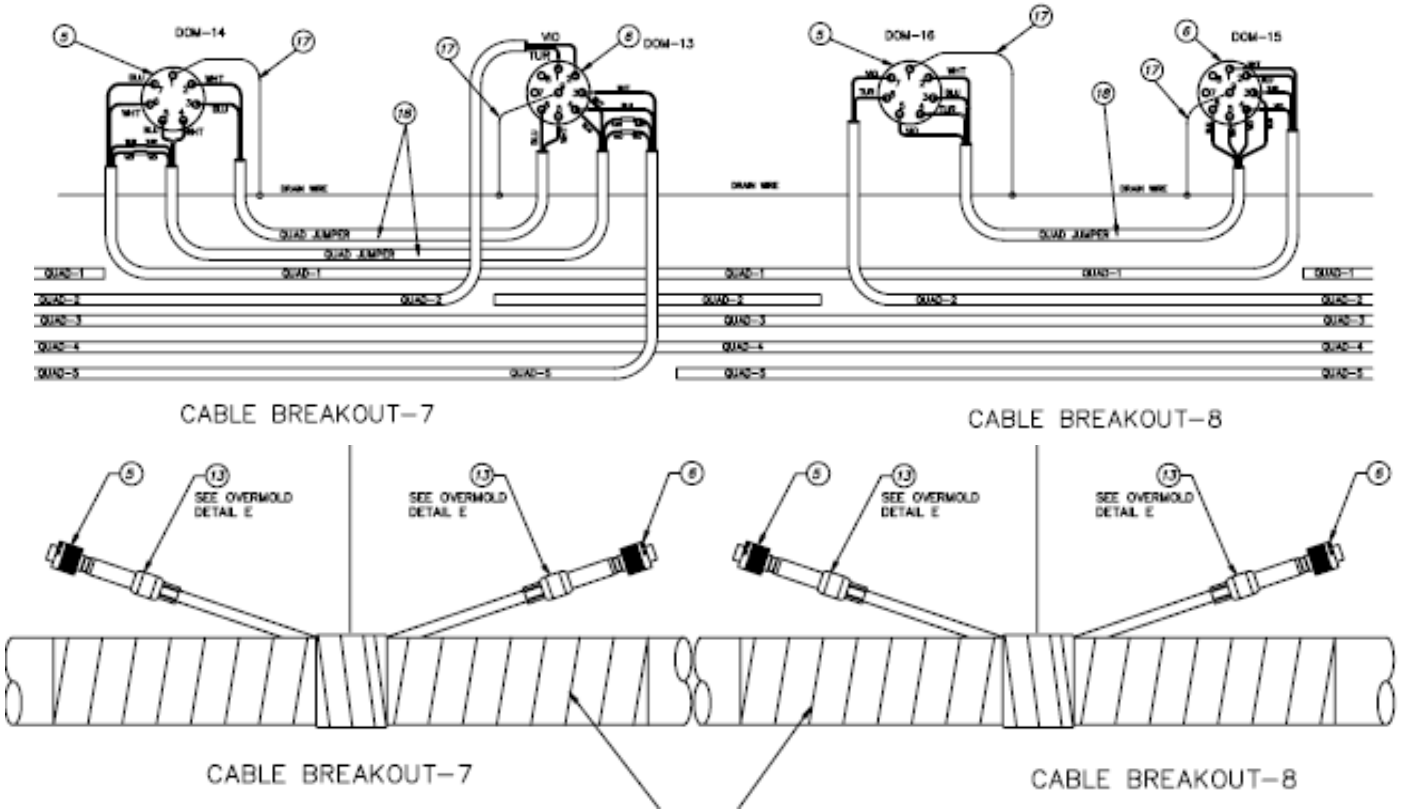
Photo by Jim Haugen

Breakout Cable Assembly (BCA) Detail



Removing LC eliminates a lot of complexity

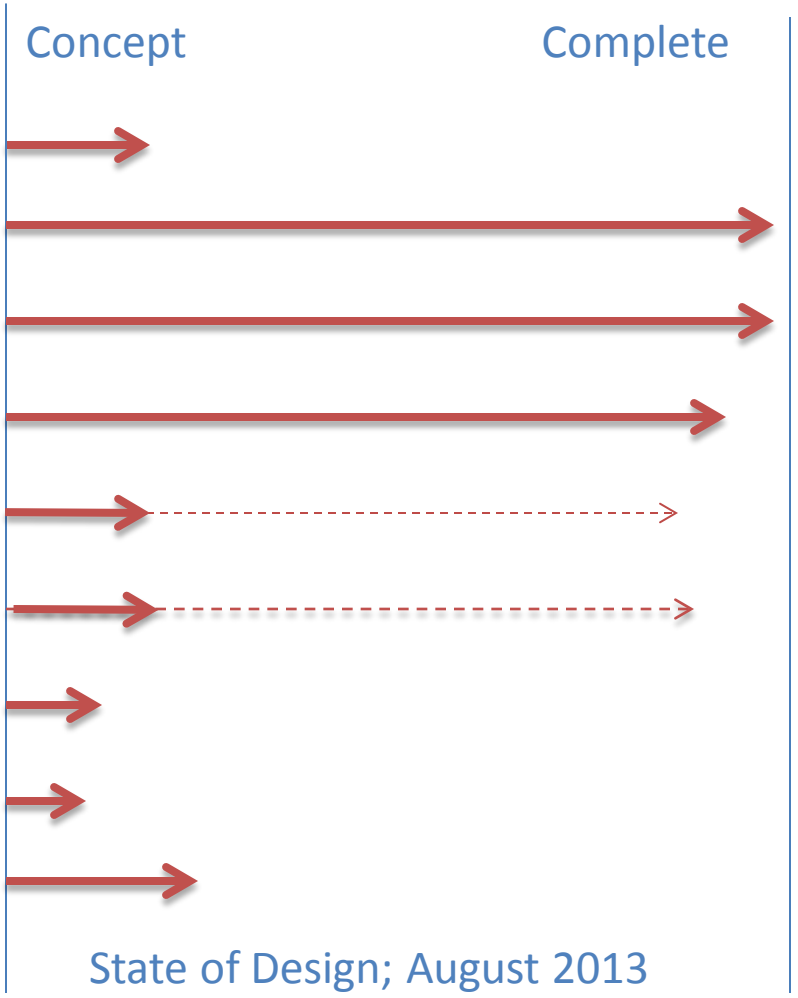
- Raw cable was significantly modified to make down-hole cable assembly for IceCube
- Internal quads are used for all LC jumpers
- Each breakout is hand-sliced and soldered to XSJJ connector pigtails
- Significant Cost/Risk reduction despite engineering of all new cable assemblies



PINGU INSTRUMENTATION R&D

(Includes efforts from IceCube)

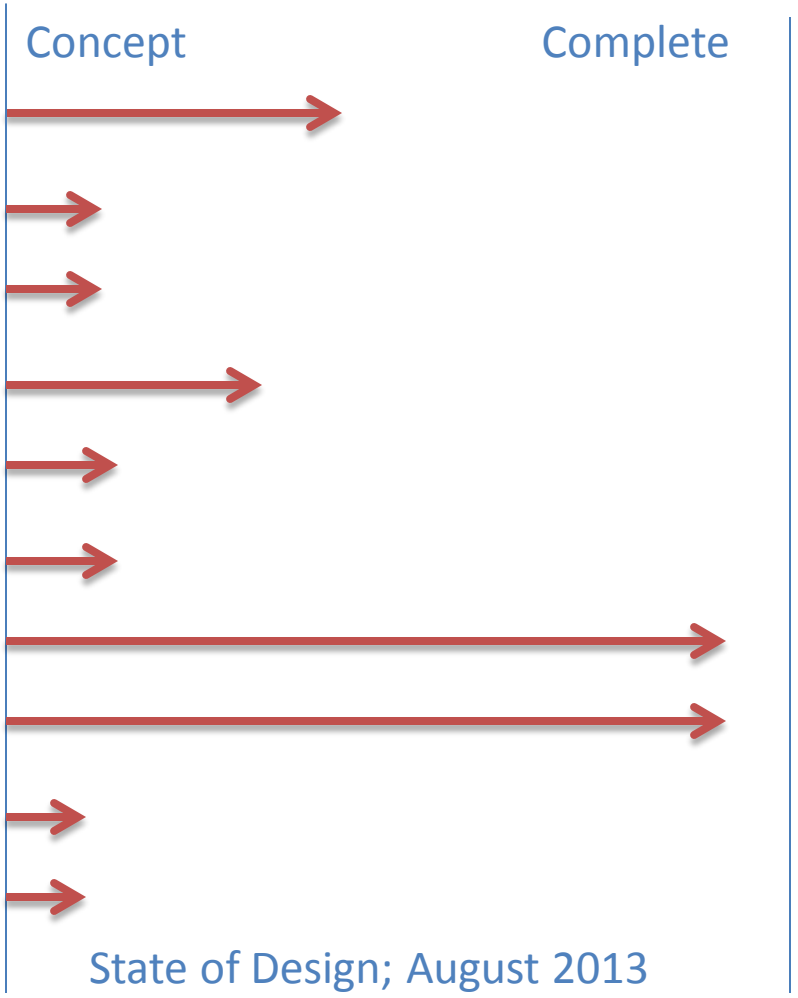
	FTE-Yrs
• PDOM Electronics	6.0
• PDOM PMT/optical	2.0
• PDOM Mechanical	3.0
• PDOM Penetrator	0.2
• Cable Downhole	4.0
• Cable Surface	4.0
• Cable Breakout Assy	0.3
• Surface DAQ	4.0
• Surface Clk. Dist.	0.6



PDOM Electronics Design (HW,FW,SW)

(Includes efforts from IceCube)

	FTE-Yrs
• Digitizer	1.0
• Front End	0.3
• Comms/Rapcal	1.0
• Oscillator	0.3
• FPGA-Processor	0.8
• LV Supply	0.5
• HV Supply	0.8
• PMT Divider	0.6
• Flasher	0.8
• BOM, DFM, DFT, etc	0.6



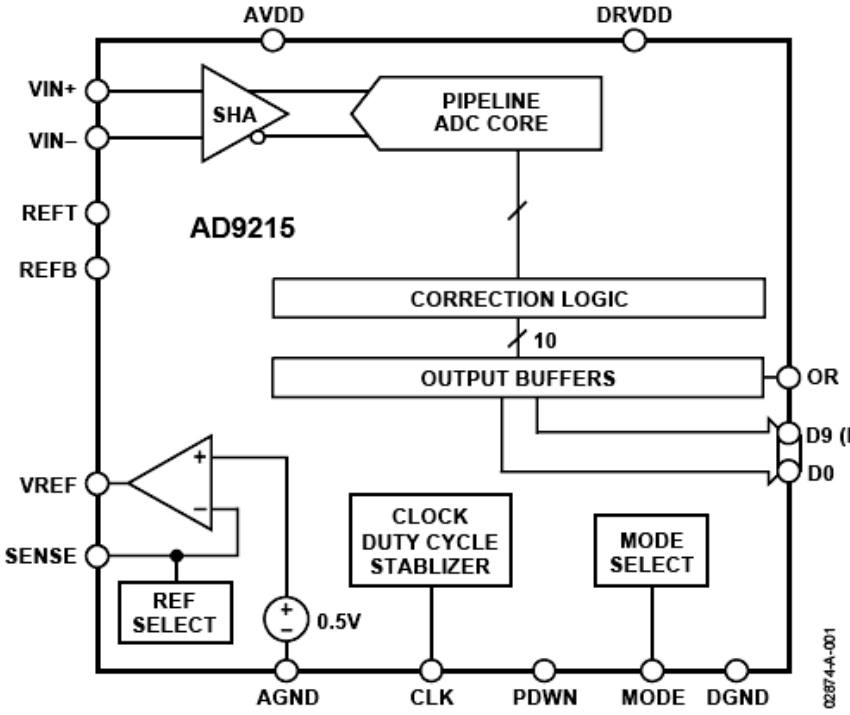
Communications Basic Requirements

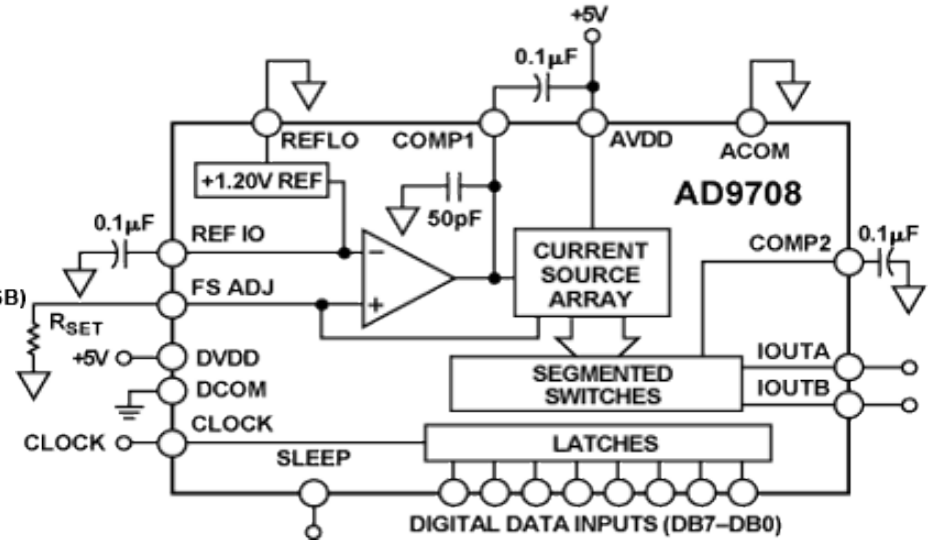
- Low Power
  - e.g. < 0.5W
- Bit Rate >= 1Mbit/second
  - Similar to IC Bandwidth but half the data
- Half-duplex operation
- ADC performance >= 10 bits & 65MS/s
  - RAPCAL/comms at least as good as IceCube
- DAC performance >= 8 bit & 125MS/s
  - RAPCAL/comms at least as good as IceCube
- Good interface, packaging , availability
- Compatibility with RAPCAL and DRAPCAL?

Comms Converters (Old IC DOM)

Baseline for Comms

- RxADC: AD9215BRU 65MSPS/10b/96mW
- TxDAC: AD9708AR 125MSPS/8b/175mW





HV Generator Basic Requirements

- Low Power
  - e.g. < 0.5W
- 12 bit setpoint resolution
  - Comparable performance to IceCube
- 0-2048V programmability
  - Comparable performance to IceCube
- Positive Output
  - Same as IceCube unless shown better otherwise
- Hi Reliability
- Low Noise
- Baseline: Same HV Supply Design as IceCube DOM

LV Supply Basic Requirements

- High Efficiency
  - e.g. > 85%
- High reliability
- Vout= 3.3V, 1.8V
- Low radiated noise
- Low conducted noise onto wire pair
- Baseline:
  - Same DC-DC Converter as IC DOM
  - New Buck step down regulation
  - Different input-side filter components

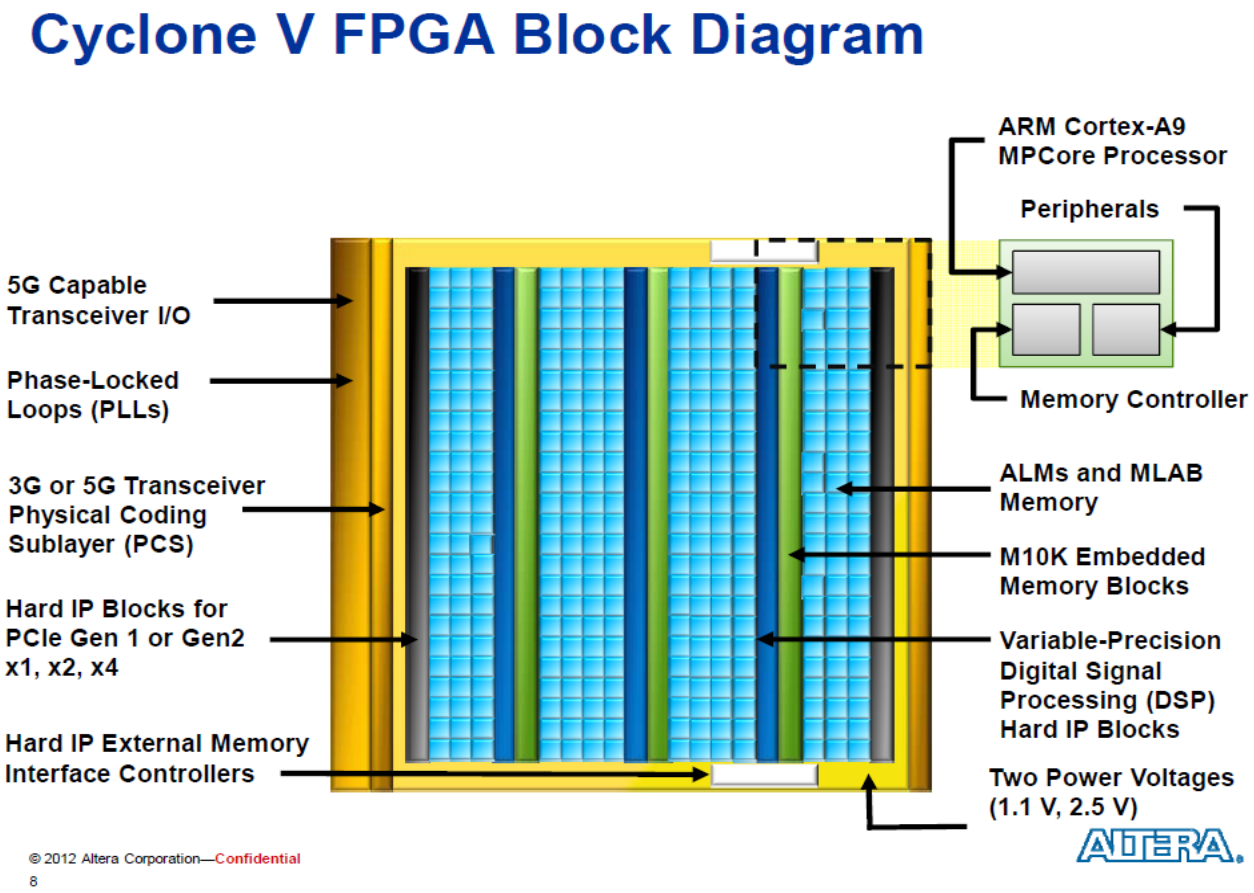
Flasher Basic Requirements

- Low Power
  - e.g. < 0.5W when active
- Good dynamic range
  - From SPE to levels similar to IC flasher
- Well-determined timing of light pulse
  - Within ~1ns w.r.t. local PDOM clock
- Pulse times programmable
  - e.g. on DOM clock edges (25ns)
- Wavelength: 370nm
- Over-illumination failsafe mechanism
- Either incorporated on MB or small Daughter Board(s)
- Emission pattern: under discussion in Pingu Cal. Group

Logic and Processor Basic Requirements

- Low Power
  - e.g. < 1W (Firmware dependent)
- High enough performance for feature extraction
- Altera Cyclone V 150K LE is baseline
- Possibly use ARM SOC version

Altera Cyclone V ; *with ARM* SOC



Cyclone 5E Standard FPGA w/NIOS (softcore) available ($20/25kLE - $250/300kLE)
(5CEA7- 150kLE available now in industrial temp range ~$200)

Cyclone 5 with Hardcore processor (SOC) available this month

IceCube DOM

PINGU DOM